Standardization of ITER Instrumentation and Controls based on Hardware Cataloges

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Outline

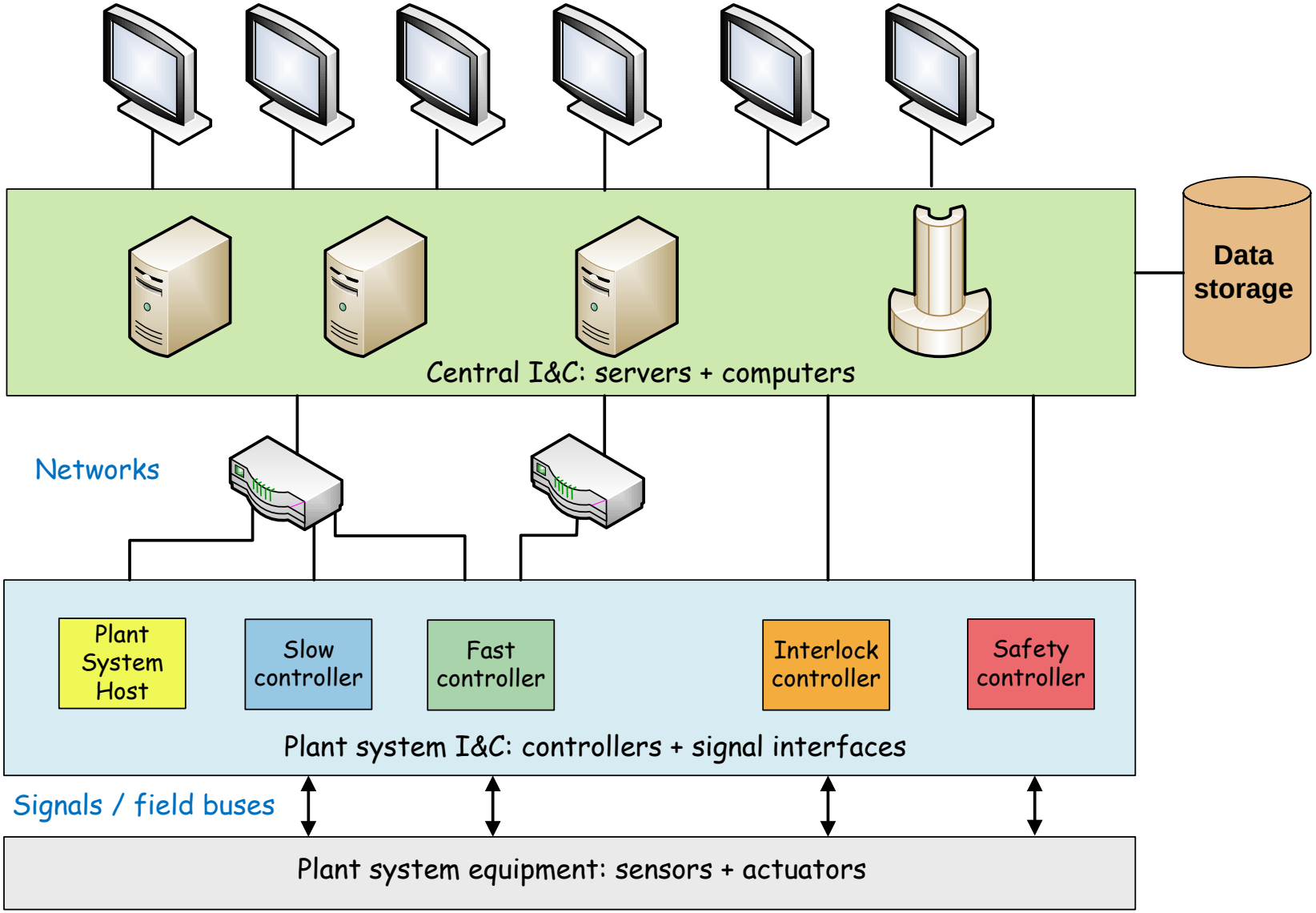
- Motivation
- Control System Architecture
- Plant I&C Standards and Development Guidelines
- Fast Controller Needs for Diagnostics
- Fast Controller Catalog
- Adding Components to the Catalog
- Conclusion

Motivation

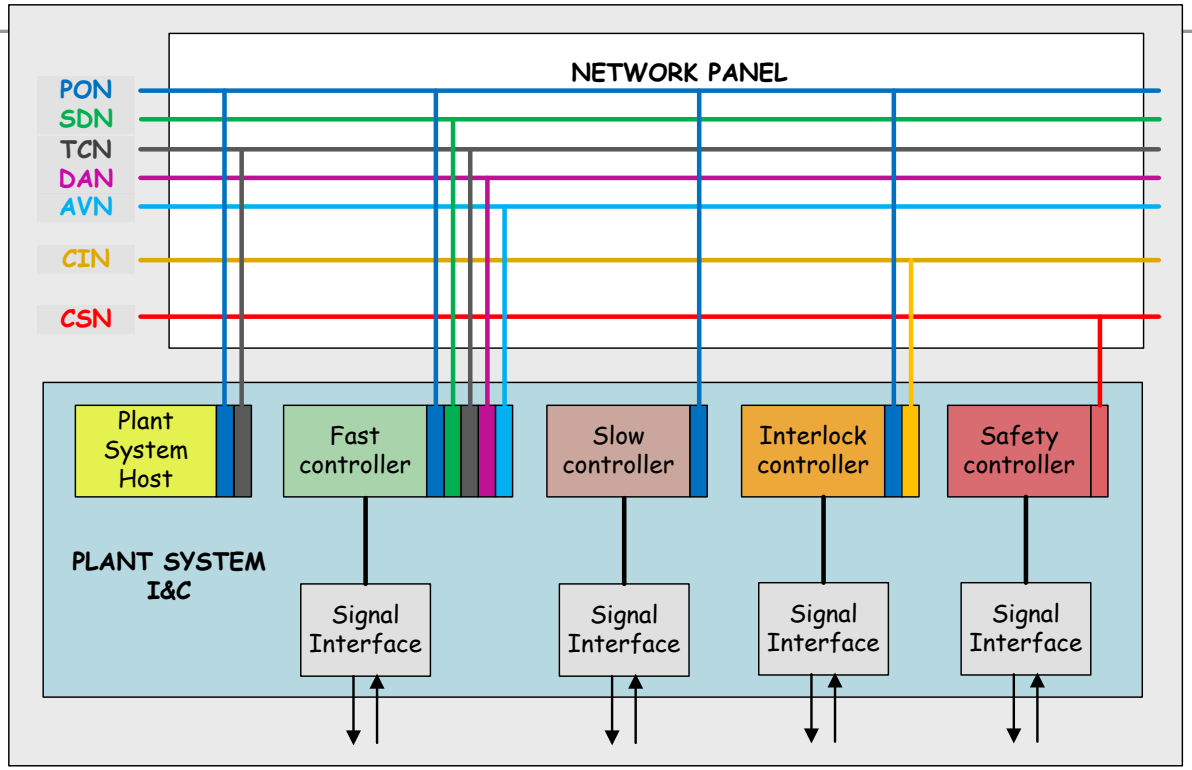
- The ITER projet's long time span and nature of I&C procurement procedures dictate that the ITER Organization defines and follows well recognized standards used both by industry and in physics experiments
  - including computer bus specification for IO devices, CPUs, etc.
  - covering electrical and mechanical aspects
  - Defining interconnection protocols between subsystems
  - support selected formfactors and commercial products for chassis, CPU, I/O and communication modules.

- I&C standards are essential for ITER to:
  - Integrate all plant systems in one control system.
  - Maintain all plant systems after delivery acceptance.
  - Contain cost by economy of scale.

Control System Architecture

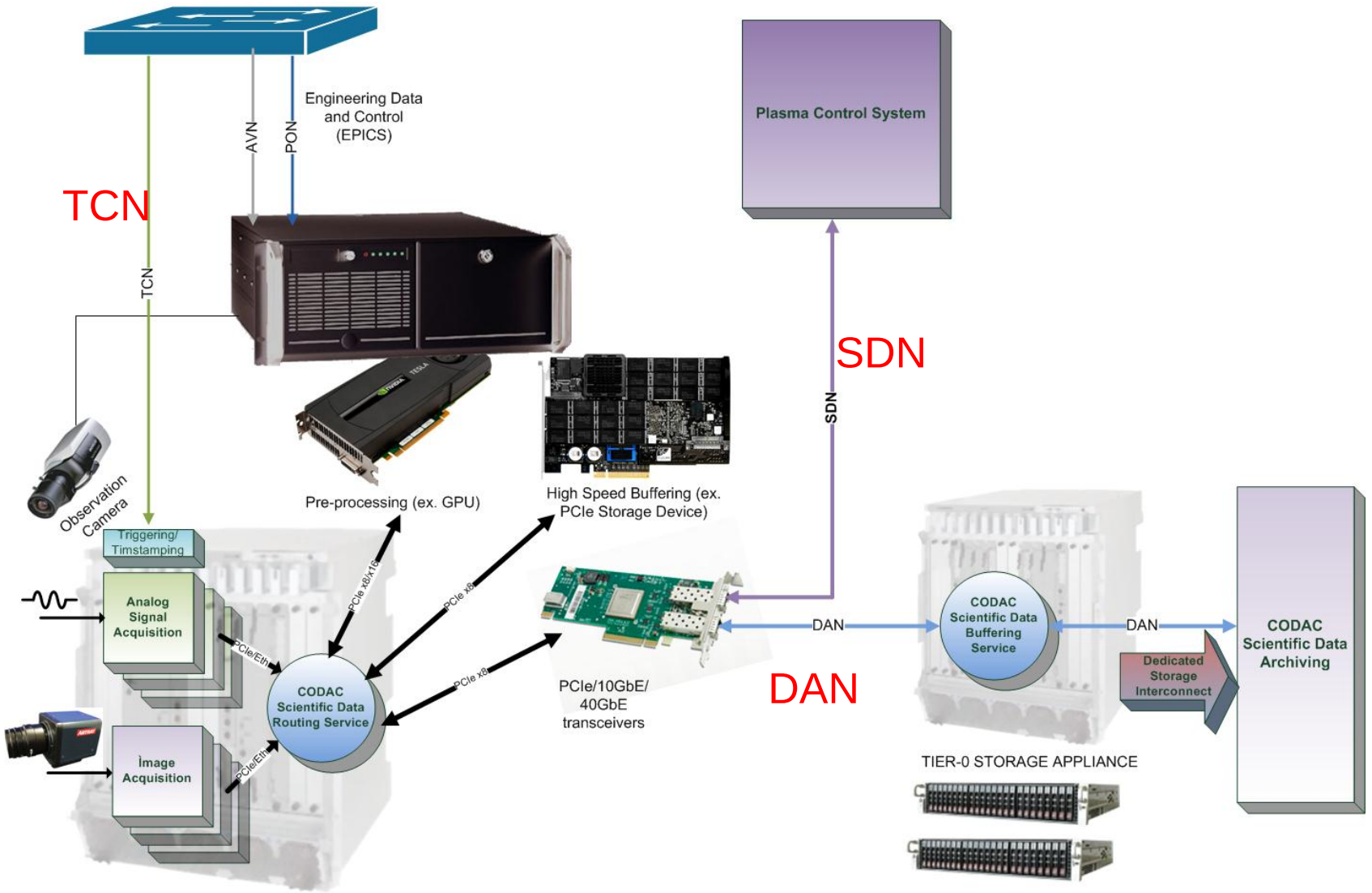


Network Interfaces

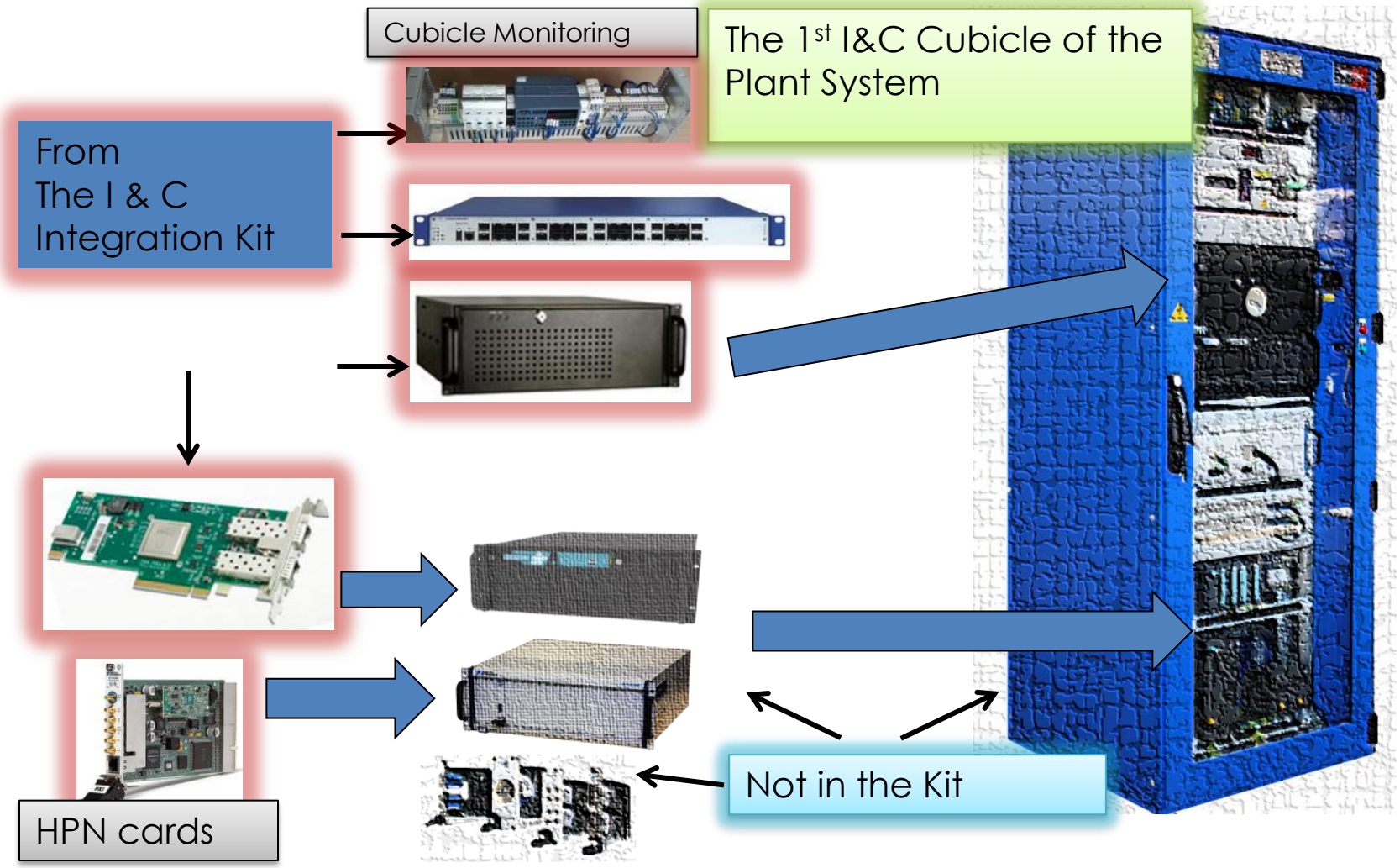


- ✓ Plant Operation Network (PON): **Industrial Ethernet**
- ✓ Synchronous Databus Network (SDN): **UDP multicast on 10 Gb Ethernet**
- ✓ Time Communication Network (TCN): **PTP, IEEE 1588**
- ✓ Audio-Video Network (AVN): **10 Gb Ethernet**
- ✓ Data Archiving Network (DAN): **10 Gb Ethernet**
- ✓ Central Interlock Network (CIN): **Industrial Ethernet**
- ✓ Central Safety Network (CSN): **Industrial Ethernet + Hard Wires**

High Performance Network Connections



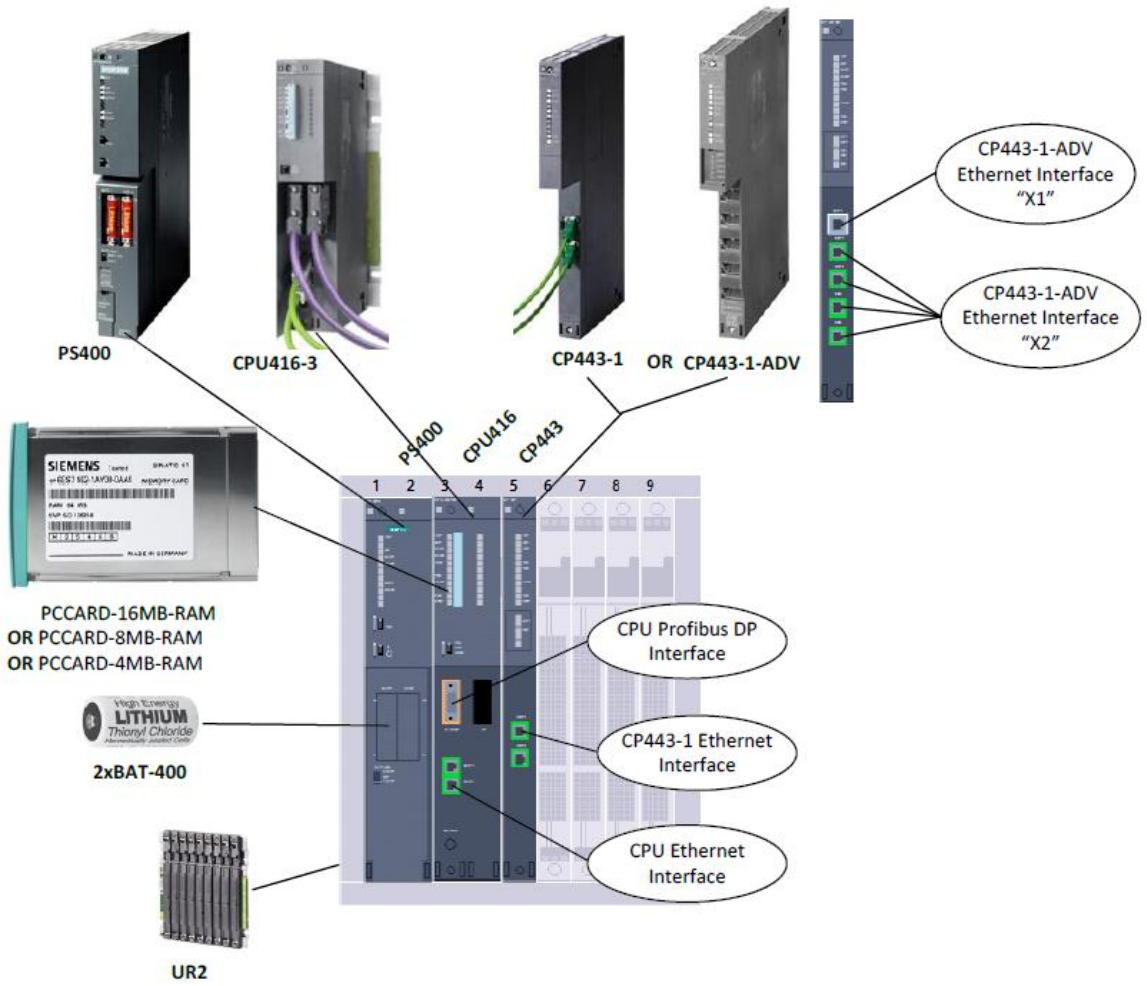
I&C Integration Kit



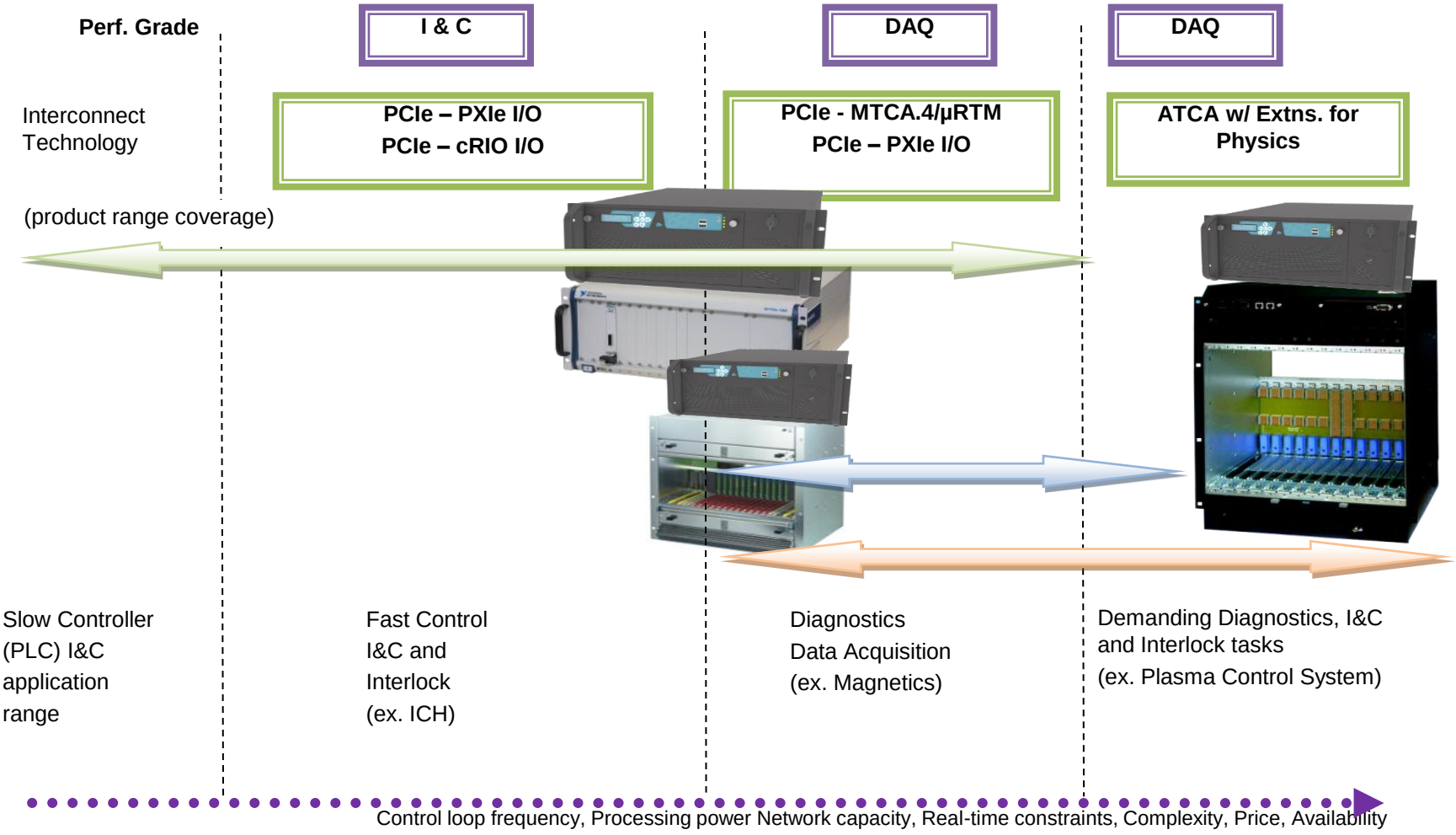
Slow Controller Standard

- ✓ Are Siemens S7-300 and S7-400 products
- ✓ Are ET200M and ET200S for Remote IO
- ✓ Are covering standard ITER signals

Slow controllers are addressing industrial controls, fail safe controls and redundant controls.



Fast Controller Standards



How to procure ITER Standards for I&C

Standard	Procedure to apply for ordering	Strategic agreement in place
CODAC Core Systems	http://www.iter.org/org/team/chd/cid/codac/coresystem	**No, CCS subscription required only,** free of charge
Slow controllers	Siemens S7 PLC ordering process for EU DA - IO standards for I&C products	**Yes** with Siemens including a special ITER discount
Cubicles	http://www.iter-schneider-electric.com/	**Yes** with Schneider-Electric including a special ITER discount
Fast controllers	Check product references in the catalogue: Fast Contollers (345X28) and order to the right supplier.	**In preparation**

How to use ITER standards for I&C

- ✓ Guidelines for ITER operator user interface (3XLESZ)
- ✓ Guidelines for ITER alarm system management (3WCD7T)
- ✓ Guidelines for PON archiving (B7N2B7)
- ✓ Guidelines for Plant system operating state management (AC2P4J)
- ✓ PLC software engineering handbook (3QPL4H)
- ✓ Guidelines for diagnostic data structure and plant system status information (354SJ3)
- ✓ Guidelines for fast controllers (333K4C)
- ✓ Guidelines for I&C signal interface (3299VT),
- ✓ Guidelines for I&C cubicle configuration (4H5DW6)
- ✓ Guidelines for PIS design (3PZ2D2)
- ✓ Guidelines for PIS integration and configuration (7LELG4)
- ✓ Guidelines for PSS design (C99J7G)

Fast Controller Needs ITER Diagnostics

Summary of Diagnostics Fast Controller Needs

- ~15000 fast ADC (1 MS/s – 1 GS/s) channels
- ~ 300 camera interfaces
- ~ 10000 digital IO
- ~ 500 timing receivers
- ~ 250 real-time network interfaces
- ~ 250 archiving network interfaces
- FPGA, GPU and CPU processing of data
- ~ 500 IO chassis with PCIe uplink to external CPU
- Formfactor PXIe, ATCA, MTCA.4
- Installed in ~ 350 racks in diagnostics building

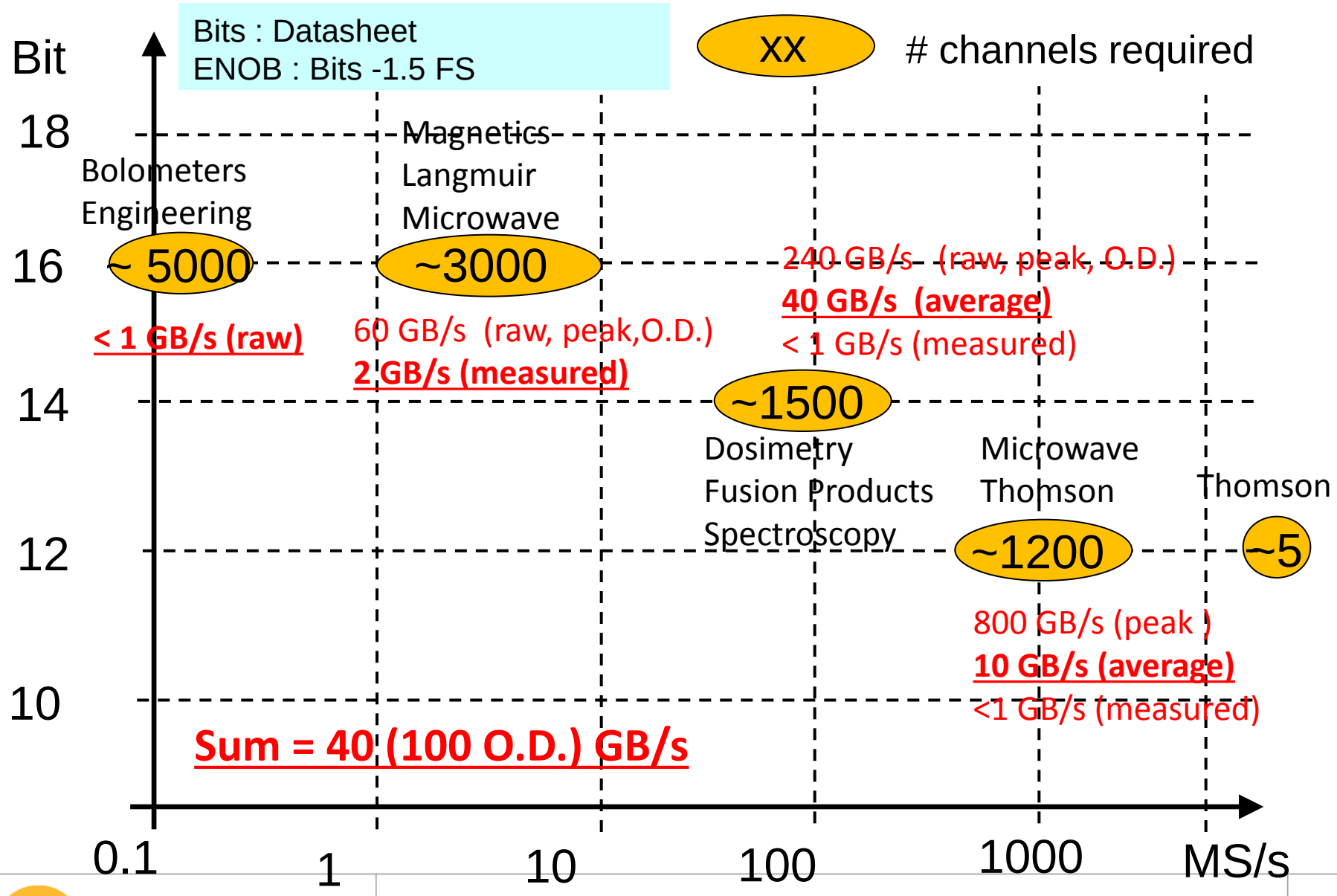
Note: For slow IO (< 100 Hz) needs ITER will use Siemens S7 PLCs. However some channels will be implemented in fast controller for cost optimisation

Basic Diagnostic Needs for I&C

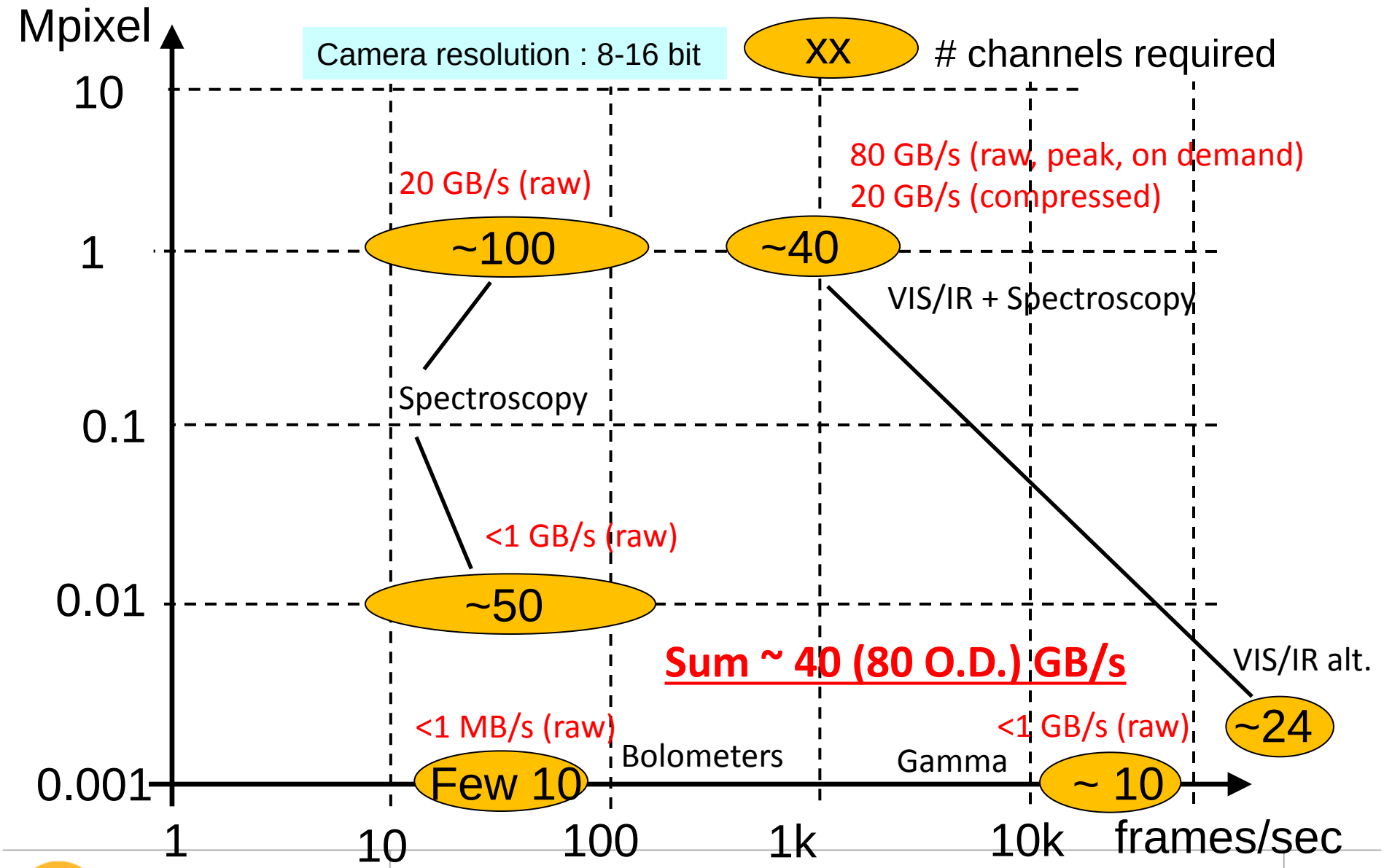
- Data Acquisition
  - 1 MS/s ADCs (16+ bit resolution, 16+ ch.)
  - 10 MS/s ADCs (16 bit resolution, 10 ch.)
  - 100 MS/s ADCs (14+ bit resolution, 10 ch.)
  - 1 GS/s (12 bit resolution, 4 ch.)
  - (Digital) Frame Grabber for Cameras (full CameraLink)
- Signal Processing
  - FPGA
  - DSP
  - CPU
  - GPU
- Communication Links
  - PCI express (PCIe)
  - Gigabit Ethernet (GbE)

Note: Covers most diagnostics fast controller needs

Estimate of ADC channels and Data



Estimate of Cameras and Data



Fast Controller Catalog

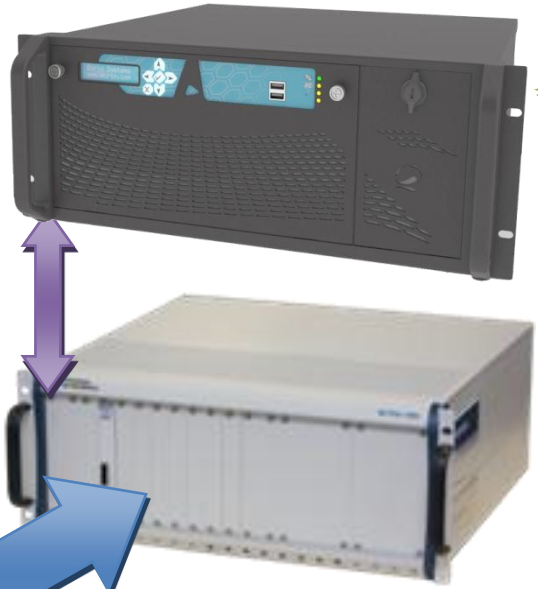
General Purpose – Standard Fast Controller

CPU/Network chassis:
- 4U PICMG 1.3

1 Gb/s Ethernet PON

Optional SDN/DAN
10 Gb/s Ethernet

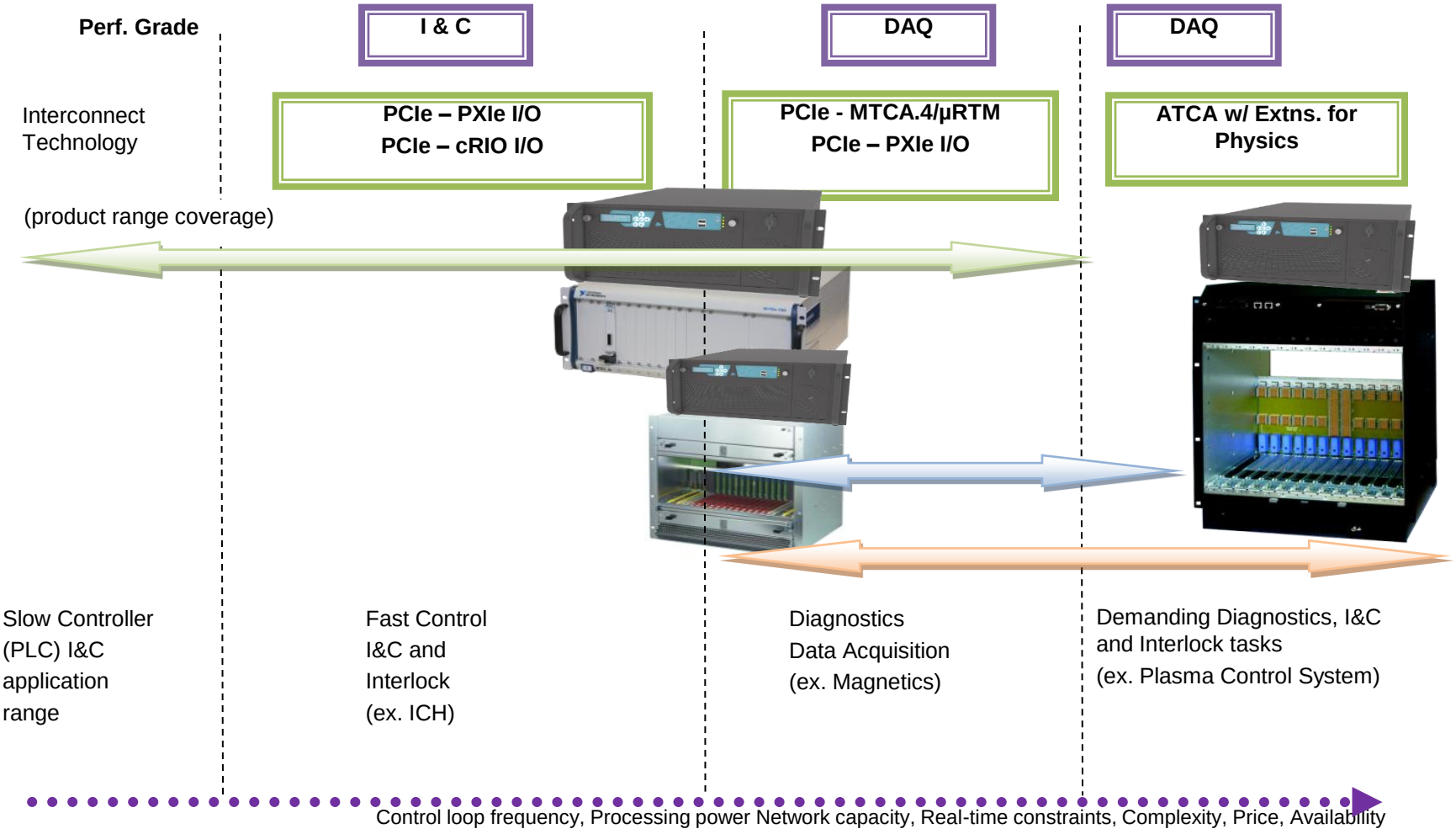
Bus Extension
PCI-Express x1



I/O Chassis:
- PXIe-1065

I/O from catalog:
- PXI
- CompactPCI
- PXI Express

Categorizing Fast Controllers



Support Categories (1)

SIG.IF	*Explanation*
PCDH	A signal interface solution is available and explained in details in **Error! Reference source not found.** and in datasheets
PLAN	A signal interface solution is required and the solution is under planning by the IO
N/R	There is no need for a signal interface solution
3RD	A signal interface solution is required and there is an adequate 3rd party solution
N/A	A signal interface solution is required but there is no known solution available

Table 1 - SIG.IF - Signal Interface Support Categories

CABLE	*Explanation*
PCDH	A cabling solution is available and explained in details in **Error! Reference source not found.** and in datasheets
PLAN	A cabling solution is under planning by the IO, in collaboration with the manufacturer or 3rd party
N/A	A cabling solution is required but the IO will not plan it
N/R	There is no need for a cabling solution

Table 2 - CABLE – Cabling Solution Support Categories

THERM	*Explanation*
PCDH	A thermal analysis and instructions related to the unit's cooling are available and explained in details in **Error! Reference source not found.** and in datasheets
PLAN	A thermal analysis is under planning by the IO, in collaboration with the manufacturer or 3rd party
N/A	A thermal analysis is required but the IO is not planning to accomplish it
N/R	There is no need for a thermal analysis

Table 3 - THERM – Thermal Analysis Categories

Support Categories (2)

RELBTY	*Explanation*
PCDH	Reliability statistics from the manufacturer are available and they are collected in datasheets so that they can be used to calculate the overall system reliability according the ITER requirements
PLAN	The IO is in process to acquire and format the reliability statistics for the item.
N/A	The IO does not plan to provide the reliability statistics for the item.
N/R	The reliability statistics are not relevant for this item.

Table 1 - RELBTY – Reliability Statistics Categories

MAGFLD	*Explanation*
PCDH	Analysis of the module's resistance in variable magnetic fields is available and explained in detailed datasheets
PLAN	The experiment or purchase of the magnetic field resistance information is under planning by the IO
N/A	The magnetic field information might have some importance but currently the IO has no plans to make the tests with this item
N/R	There is no need for the magnetic field information

Table 2 - MAGFLD – Magnetic Field Analysis Availability Categories

RADFLD	*Explanation*
PCDH	Analysis of the module's resistance under predicted radiation levels is available and explained in detailed datasheets
PLAN	The experiment or purchase of the predicted radiation level resistance analysis is under planning by the IO
N/A	The radiation level resistance information could be considered useful but the IO has no plans for the time being to obtain it
N/R	There is no need for the radiation level resistance information

Table 3 - RADFLD – Radiation Resistance Analysis Availability Categories

Software Support Categories

SOFTWARE	Explanation
CCS	The device is fully supported in CODAC Core System software (SDD, EPICS device support, Health Management, Linux device driver support w/ a specified FPGA binary, when applicable). User's Guide is available in CCS documentation set. CODAC support (ex. codac-support@iter.org) available only at this level.
BETA	All of the same elements as with CCS level category are available at beta quality level, for a manual installation, installing also the documentation in the local file system from an ITER repository (*i.e.* RPMs in SVN or codac-dist). At this level, no CODAC support is available by default but it can be arranged case by case, please contact the author of this document directly to get the links to the software and documentation.
ALPHA	Some software support exists but not at CODAC Core System quality level, only at alpha quality level. For example, only the Linux support may be available but no EPICS support. Also, the documentation does not have to be completely available. The availability of the software on the ITER repository server is not mandatory but a working, CCS-compatible packaging (mvn, rpm) for RHEL 6.x is mandatory even in this category. No CODAC support is available by default but it can be decided, case by case to leverage the software to the beta level. To start with a ALPHA level software, please contact the author of this document directly to get the links to the software and documentation.
N/R	There is no need for software support.

Examples from Catalog (1)

5.1 I&C Grade PICMG 1.3 PC 4U Computer

Manufacturer's Reference	*Short Form Description*	*ITER Reference and Datasheets*
ID01549-A-001/ITER	PICMG 1.3 (PCIe 3.0), 2 x Xeon = 8 cores, 8 GB DRAM, 2xSSD(RAID-1)	BKLT5Z
ID01549-B-001/ITER	Same as above but with 16 GB + NVIDIA Quatro 400 GPU + Drive bay (w/o extra disks)	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PLAN**	**PCDH**	**PLAN**	N/R

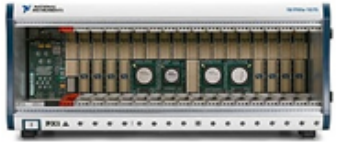
5.2 DAQ Grade PICMG 1.3 PC 4U Computer

Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
ID01550-A-001/ITER	PICMG 1.3 (PCIe 3.0), 2 x Xeon = 16 cores, 24 GB DRAM, 2xSSD(RAID-1)	BNXX8V
ID01550-B-001/ITER	as above but 32 GB + NVIDIA GTX680GPU(Kepler)	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PLAN**	**PCDH**	**PLAN**	N/R

Examples from Catalog (2)

6.3 DAQ Grade PXI Express I/O Chassis Solutions



Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
PXIe-1075	4U/19 inch rackable, 18 3U Slots (8 hybrid slots, 8 PXI Express slots (PCI Express V1.1), 1 PXI Express system timing slot) w/ front rack mounting kit, EMC filler kit, cable management (**4 GB/s**)	C2LAG7
PXIe-1085	5U/19 inch rackable, high-speed version of the PXIe-1075, w/ AC power supply, swappable fans.	
PXIe-PCIe8388	Remote PCI Express x16 (v2.0) Control of PXI Express **5.6 GB/s**	
PXIe-PCIe8389	Same as above w/ dual port at PXIe for daisy-chaining of two chassis **5.6 GB/s**	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PCDH**	**PCDH**	**PCDH**	PLAN

6.4 DAQ MTCA.4 I/O Chassis Solutions

Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
039-362	MTCA.4 8U 84HP 12 slots	C3DEPW
PUMA 900W	Power supply	
NAT-MCH	Carrier Hub MCH	
MPCIE-16-FS	MTCA.4 to PCI Express Switch PCI Express v3.0	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PCDH**	**PCDH**	**PCDH**	PLAN

Examples from Catalog (3)

7.1 Timing, synchronization and triggering solutions

In each Fast Controller, at least one of the presented I/O modules will be connected to the ITER CODAC Time Communication Network (TCN).

7.1.1 I&C PCI, PXI and PXI Express Timing, Synchronization and Triggering

Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
PXIe 6683H	PXIe Hybrid slot compatible triggering (no PXIe star-lines) and clock generation, timestamps, synchronizing with ITER CODAC TCN. *Delivered 3Q2013 onwards (CCS v4.1)*	C62B6C
PXI 6682	PXI version of the PXIe-6683H *Delivered until end of 2Q2012 (CCS v4.0) only*	
PCI-1588	PCI synchronizing with ITER CODAC TCN. Delivered for Fast Controllers with no I/O (ex. Master Controllers). Obsolete, phased out in 2013, reference ID01549-A-001/ITER (5.1) is compatible with TCN.	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PCDH**	**PCDH**	**PCDH**	PLAN

Examples from Catalog (4)

7.2 Data Archiving and Synchronous Databus Connectivity

This section specifies the I/O modules for interfacing with ITER CODAC Synchronous Databus Network (SDN) and Data Archiving Network (DAN). Since the base technology is based on 10 GbE it is recommended to use these products wherever the 10 GbE optional Ethernet interconnect is required.

7.2.1 DAQ PCI Express DAN and SDN Connectivity Solutions

Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
S310E-CR	Single port 10GbE T3 Adapter for PCI Express x8	C8J4JW
S320E-CR	Dual port 10GbE T3 Adapter for PCI Express x8	
SM10G-LR	10 G long reach single-mode optical module	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	PLAN	PCDH	PLAN	PLAN

Examples from Catalog (5)

8.3 DAQ Grade PXI Express I/O Boards and Bundles

Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
PXIe 6368	32 x AI (16-bit, ±10V, ±5V, ±ext ref) **2 MS/s** (simultaneous) 4 x AO (16-bit, ±10V, ±5V, ±ext ref) **3.3 MS/s** (simultaneous) 48 x DIO (CMOS TTL 24mA), 32 lines are clocked, **10 MHz** max.	C8TQ8R
ADQ412-3G-PXIe	2/4 x AI (12-bit) **3.6 GS/s** 2 GHz	
PXIe 7966R / 5761R	FPGA / ADC Bundle **250 MS/s** 500 MHz / 14-bit 4 ch + DIO	
PXIe-7961R / 6581	FPGA / DIO Bundle **100 MHz**, 54 x DIO	
PXIe 7966R / 1483	FPGA / Image Acquisition Bundle Camera Link (10-tap, 80-bit images) 20 to 85 MHz pixel clock 4 TTL DO, 2 Optical DI, 1 Quadrature encoder input	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	ALPHA	**PCDH**	**PCDH**	**PCDH**	**PCDH**	**PCDH**	PLAN

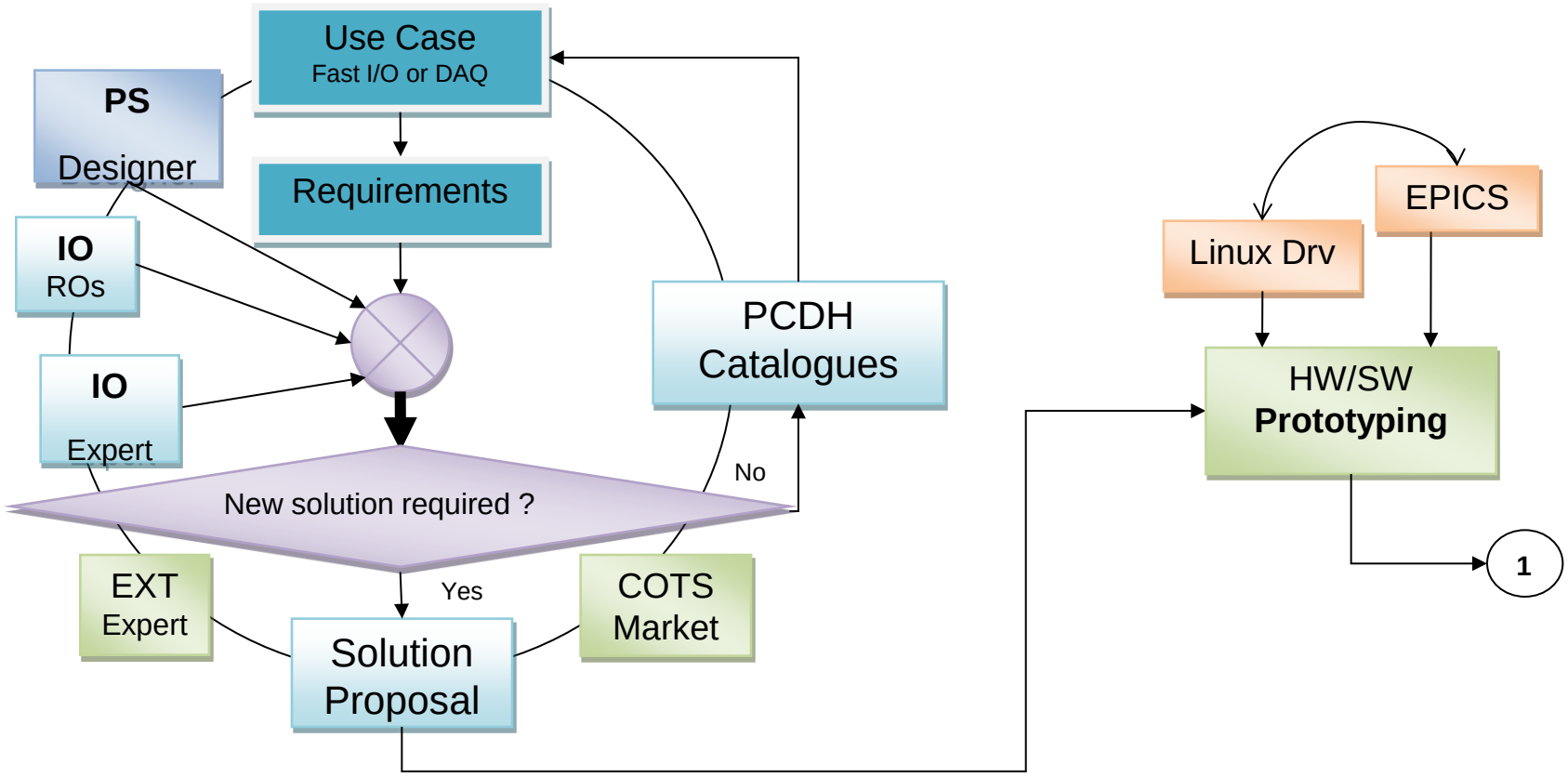
Examples from Catalog (6)

8.4 DAQ Grade MTCA.4 I/O Boards and Bundles

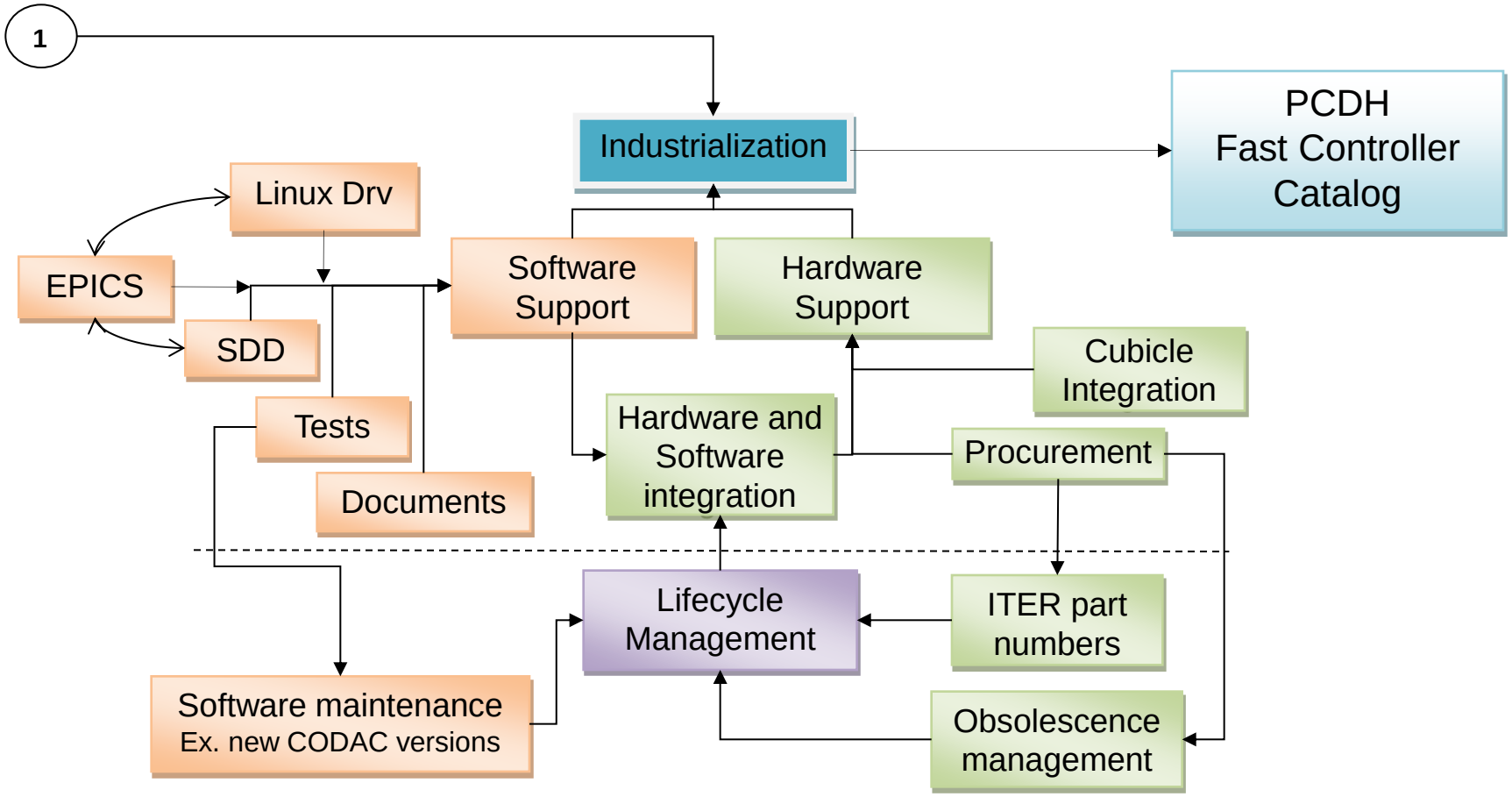
Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
SIS8300 04075 / SIS8900	10 x AI (16-bit) **125 MS/s** w/ single-ended RTM-module	C8TB4C
ADQ412-3G-MTCA	2/4 x AI (12-bit) **3.6 GS/s** 2 GHz	
SIS8300 04075 / RTM 7201	10 x AI (16-bit) **125 MS/s** 10 kHz – 1 MHz Chopper Integrator 4 channels ±5V / ±50V (50 ms) 1 kΩ, int.error < 200µVs / 1000 s	
TAMC640-12R / FMC-200	FPGA / Image Acquisition Bundle Camera Link (7.14 Gb/s) 85 MHz pixel clock	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	ALPHA	**PCDH**	**PCDH**	**PCDH**	**PCDH**	**PCDH**	PLAN

Fast Controller Catalog – New items needed



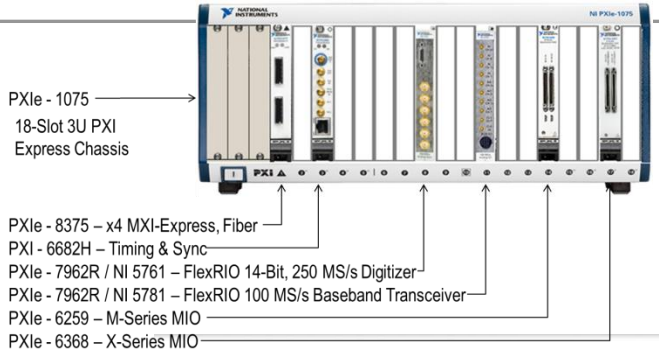
Fast Controller Catalog – Total Cost of Ownership



Magnetic and Radiation Field Testing

1.1.1 *Test Setup*

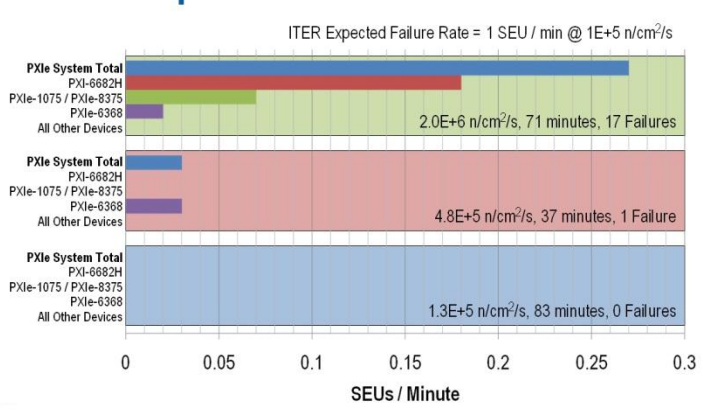
Figure 1 – PXIe Set-up in the Test Magnet

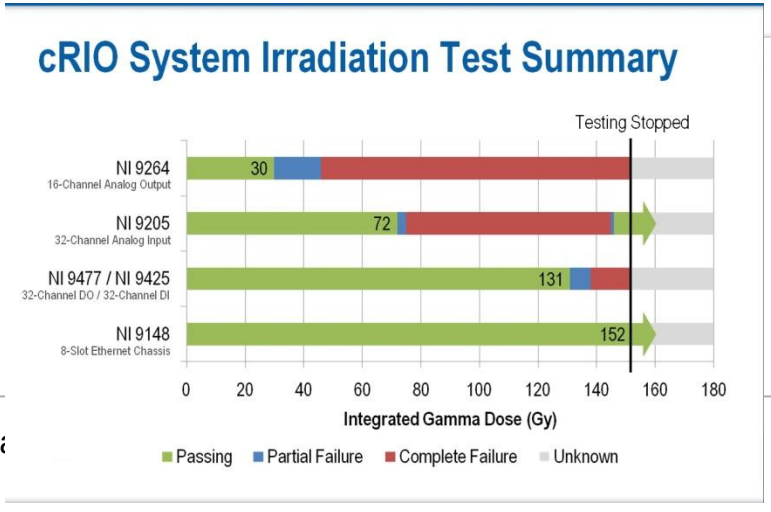


1.1.2 *Summary of PXIe Tests (PXIe IO) chassis*

B [mT]	Main Device effected	Description of Observation / Action
50	Chassis not powered	Surveyed magnetic fields. 10 mT = 10 A at magnet.
0	Chassis powered	Fully functional
10 (13)	Chassis Fan	Fan #3 speed dropped by 200 rpm due to field short overshoot to 13 mT; recovered after 5 seconds
13 - 15	Chassis Fan	Fan # 3 stops running (displays 82 rpm) Note 1: Power still ok. Note 2: Fan 3 never recovered when lowering field Note 3: Fan 3 could be mechanically jumpstarted but reading remained at 82 rpm Note 4: When power was turned off, fan 3 stopped in half time (probably less rpm) Note 5: Power supply light was red with one fan failed
13 -15	Chassis Fan	Later Fan #1 also stopped permanently. Note: With 2 fans failed the power supply shuts down
Summary:		PXIe System not operable in fields > 13 mT due to stoppage of chassis fans and resulting shutdown of power supply

Additional Notes





Conclusion

- Hardware Catalogs have been established for
  - Cubicles (Racks)
  - Slow Controllers
  - Fast Controllers
- Hardware catalogs are used by domestic agencies as a reference for plant I&C design.
- Fast controller catalog dominated by diagnostic needs.
- Diagnostic use case examples demonstrate integrated solution
- Strategic agreements in place or planned to simplify procurement